

40W - 28V - 500MHz
GOLD METALLISED MULTI-PURPOSE
SILICON DMOS RF FET

FEATURES

- METAL GATE
- EXTRA LOW C_{rss}
- BROAD BAND
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS
from DC to 850 MHz

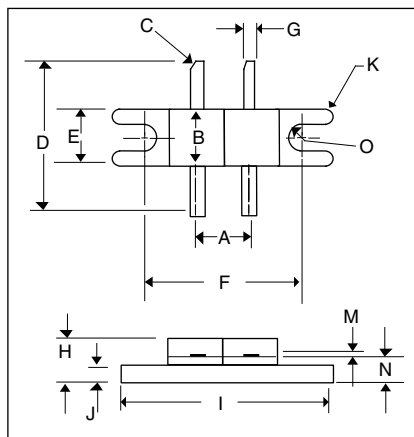
ABSOLUTE MAXIMUM RATINGS
($T_{CASE} = 25^{\circ}C$ unless otherwise stated)

P_D	Power Dissipation	175W
BV_{DSS}	Drain-source breakdown voltage	70V
V_{GSS}	Gate-source voltage	$\pm 20V$
I_D	Drain Current	10A
T_{stg}	Storage temperature	65 to $150^{\circ}C$
T_j	Maximum operating junction temperature	$200^{\circ}C$
$R_{THj-case}$	Thermal resistance junction-case	Max. $1.0^{\circ}C/W$

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<u>PER SIDE</u>					
BV_{DSS}	Breakdown voltage, drain source $V_{GS}=0$ $I_D=100mA$	70			Vdc
I_{DSS}	Drain leakage current $V_{DS}=28V$ $V_{GS}=0$			2	mAdc
I_{GSS}	Gate leakage current $V_{GS}=20V$ $V_{DS}=0$			1	μ Adc
$V_{GS(th)}$	Gate threshold voltage $I_D=10mA$ $V_{DS}=V_{GS}$	1		7	Vdc
g_{fs}	Transconductance (300 μ s pulse) $V_{DS}=10V$ $I_D=2A$	1.6			Mhos
<u>TOTAL DEVICE</u>					
G_{PS}	Common source power gain $P_o=40W$	13			dB
η	Drain efficiency $V_{DS}=28V$ $I_{DQ}=0.8A$	50			%
VSWR	Load mismatch tolerance $f=500MHz$	20:1			
<u>PER SIDE</u>					
C_{iss}	Input capacitance $V_{DS}=0V$ $V_{GS}=-5V$ $f=1MHz$			120	pF
C_{oss}	Output capacitance $V_{DS}=28V$ $V_{GS}=0$ $f=1MHz$			60	pF
C_{rss}	Reverse transfer capacitance $V_{DS}=28V$ $V_{GS}=0$ $f=1MHz$			5	pF

DIMENSIONS



DM	Millimeter	TOL	Inches	TOL
A	6.45	.13	.254	.005
B	6.35	.13	.250	.005
C	45°	5°	45°	5°
D	16.51	.76	.650	.030
E	6.48	.13	.255	.005
F	18.42	.13	.725	.005
G	1.52	.13	.060	.005
H	4.83	.03	.160	.010
I	24.77	.13	.975	.005
J	1.52	.13	.060	.001
K	0.81R	.13	.032R	.005
M	.013	.02	.005	.001
N	2.16	.13	.085	.005
O	1.65R	.01	.065R	.005

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

U.S. PATENTS 5,121,176 & 5,179,032
GLOBAL PATENTS PENDING

*D1008 (per side)

*PSPICE MODEL FOR POINT NINE TECHNOLOGIES, Inc RF N-CHANNEL VERTICAL DMOS POWER FET
*PRELIMINARY DATA, SEPTEMBER 1995

*THIS IS A PUSH-PULL DEVICE, MODEL DATA IS PER SIDE
*TO GENERATE S PARAMETERS MATCHING DATA SHEET, SET VG=3.2V FOR IDQ=1A

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*      ____GATE
*      I      ____DRAIN
*      I      I      ____SOURCE
*      I      I      I
.SUBCKT D1008 10 20 30
LG 10 11 1.85N
RGATE 11 12 0.39
CG 10 30 0.05P
CRSS 12 17 5P
CISS 12 14 120P
LS 14 30 0.15N
CS 14 30 0.1P
LD 17 20 0.42N
CD 20 30 1.44P
R_RC 16 17 35.73
C_RC 14 16 11.8P
MOS 13 12 14 15 D1008MOS L=0.71U W=0.112664 ;D G S B LEVEL1
JFET 17 14 13 D1008JF ;D G S
DBODY 14 17 D1008DB ;P N

.MODEL D1008MOS NMOS (VTO=2.2 KP=1.8E-5 LAMBDA=0.1 RD=0.13 RS=0.25)
.MODEL D1008JF NJF (VTO=-7.5 BETA=0.04 LAMBDA=1)
.MODEL D1008DB D (CJO=177P RS=0.25 VJ=0.7 M=0.33 BV=70)
.ENDS
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D1008.s2p (each side)

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!      Vds=28V, Idq=1A
#      MHz S MA R 50
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!Freq	S11 mag	S11 ang	S21 mag	S21 ang	S12 mag	S12 ang	S22 mag	S22 ang
100	0.794	-158	14.622	69	0.0115	-7	0.61	-145
200	0.881	-167	5.821	42	0.0061	3	0.794	-156
300	0.923	-171	3.02	28	0.0068	60	0.871	-162
400	0.923	-176	1.82	18	0.117	77	0.902	-167
500	0.937	-179	1.439	15	0.0168	76	0.923	-169
600	0.952	177	1.057	13	0.0234	75	0.945	-171
700	0.966	174	0.676	10	0.0285	74	0.966	-174
800	0.966	171	0.543	5	0.0335	69	0.955	-177
900	0.977	167	0.447	1	0.0394	64	0.966	178
1000	0.966	165	0.359	1	0.0432	64	0.955	178