

10W - 28V - 500MHz
GOLD METALLISED MULTI-PURPOSE
SILICON DMOS RF FET

FEATURES

- METAL GATE
- EXTRA LOW C_{rss}
- BROAD BAND
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS
from DC to 500MHz

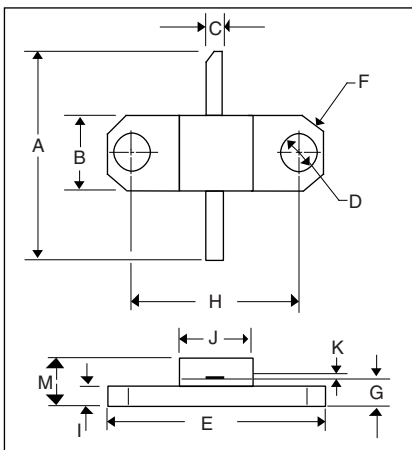
ABSOLUTE MAXIMUM RATINGS
($T_{CASE} = 25^{\circ}C$ unless otherwise stated)

P_D	Power Dissipation	50W
BV_{DSS}	Drain-source breakdown voltage	70V
V_{GSS}	Gate-source voltage	$\pm 20V$
I_D	Drain Current	2.5A
T_{stg}	Storage temperature	65 to 150°C
T_j	Maximum operating junction temperature	200°C
$R_{THj-case}$	Thermal resistance junction-case	Max. 3.5°C/W

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ unless otherwise stated)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Breakdown voltage, drain source	$V_{GS}=0$ $I_D=100mA$	70			Vdc
I_{DSS}	Drain leakage current	$V_{DS}=28V$ $V_{GS}=0$			1	mAdc
I_{GSS}	Gate leakage current	$V_{GS}=20V$ $V_{DS}=0$			1	μAdc
$V_{GS(th)}$	Gate threshold voltage	$I_D=10mA$ $V_{DS}=V_{GS}$	1		7	Vdc
g_{fs}	Transconductance (300 μs pulse)	$V_{DS}=10V$ $I_D=1A$	0.8			Mhos
G_{ps}	Common source power gain	$P_O=10W$	13			dB
η	Drain efficiency	$V_{DS}=28V$ $I_{DQ}=0.2A$	50			%
VSWR	Load mismatch tolerance	$f=500MHz$	20:1			
C_{iss}	Input capacitance	$V_{DS}=0V$ $V_{GS}=-5V$ $f=1MHz$			60	pF
C_{oss}	Output capacitance	$V_{DS}=28V$ $V_{GS}=0$ $f=1MHz$			30	pF
C_{rss}	Reverse transfer capacitance	$V_{DS}=28V$ $V_{GS}=0$ $f=1MHz$			2.5	pF

DIMENSIONS



DM	Millimeter	TOL	Inches	TOL
A	16.51	.25	.650	.010
B	6.35	.13	.250	.005
C	1.52	.13	.060	.005
D	3.30	.13	.130	.005
E	18.90	.05	.744	.005
F	1.27 X 45°	.13	.050 X 45°	.005
G	2.16	.13	.085	.005
H	14.22	.05	.560	.005
I	1.52	.13	.060	.005
J	6.35	.13	.250	.005
K	0.10	.02	.004	.001
M	5.08	MAX	.200	MAX

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

U.S. PATENTS 5,121,176 & 5,179,032
GLOBAL PATENTS PENDING

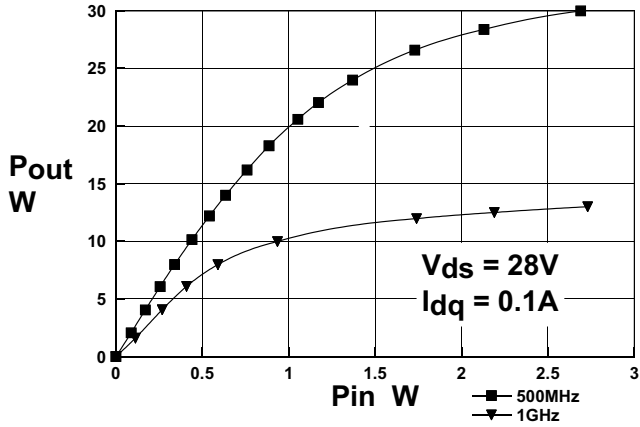


Figure 1
Power Output vs. Input Power

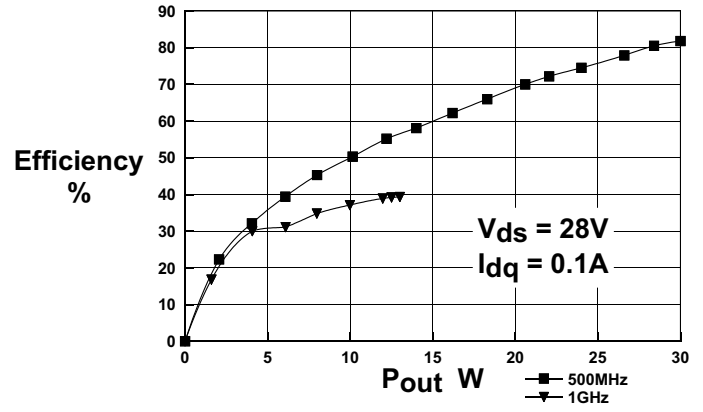


Figure 2
Efficiency vs. Output Power

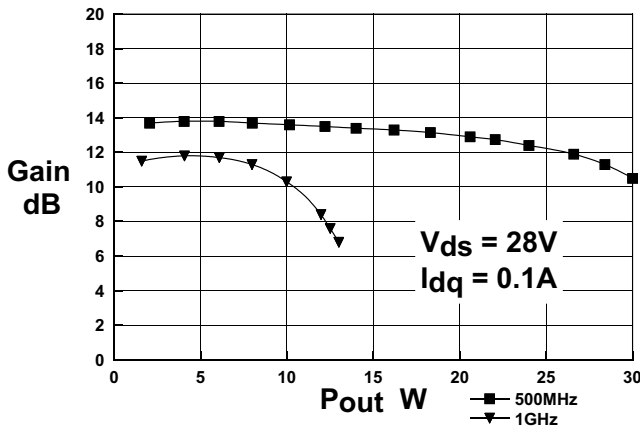


Figure 3
Gain vs. Output Power

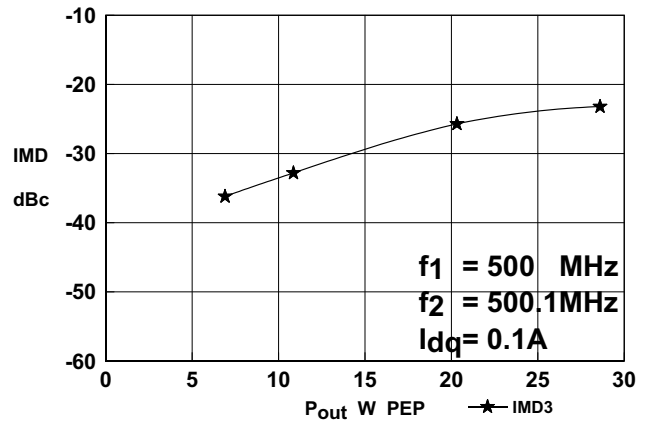


Figure 4
IMD vs. Output Power

