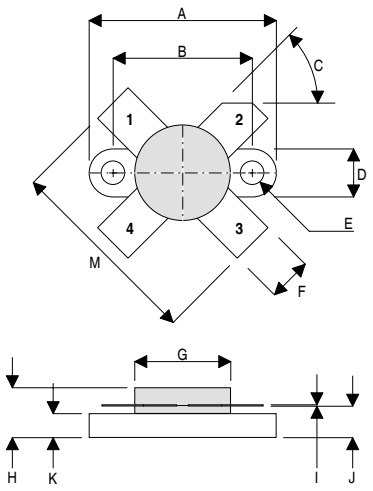
POINT NINE
Technologies, Inc.

D1017 TetraFET

METAL GATE RF SILICON FET

MECHANICAL DATA



DM

PIN 1	SOURCE	PIN 2	DRAIN
PIN 3	SOURCE	PIN 4	GATE

DIM	mm	Tol.	Inches	Tol.
A	24.76	0.13	0.975	0.005
B	18.42	0.13	0.725	0.005
C	45°	5°	45°	5°
D	6.35	0.13	0.25	0.005
E	3.17 Dia.	0.13	0.125 Dia.	0.005
F	5.71	0.13	0.225	0.005
G	12.7 Dia.	0.13	0.500 Dia.	0.005
H	6.60	REF	0.260	REF
I	0.13	0.02	0.005	0.001
J	4.32	0.13	0.170	0.005
K	3.17	0.13	0.125	0.005
M	26.16	0.25	1.03	0.010

GOLD METALIZED MULTI-PURPOSE SILICON DMOS RF FET 150W – 28V – 175MHz SINGLE ENDED

FEATURES

- **SIMPLIFIED AMPLIFIER DESIGN**
- **SUITABLE FOR BROAD BAND APPLICATIONS**
- **LOW C_{rss}**
- **SIMPLE BIAS CIRCUITS**
- **LOW NOISE**
- **HIGH GAIN – 13 dB MINIMUM**

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS from 1 MHz to 200 MHz

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

P_D	Power Dissipation	220W
BV_{DSS}	Drain – Source Breakdown Voltage	70V
BV_{GSS}	Gate – Source Breakdown Voltage	±20V
$I_{D(sat)}$	Drain Current	30A
T_{stg}	Storage Temperature	–65 to 150°C
T_j	Maximum Operating Junction Temperature	200°C

2697 Lavery Court #8 • Newbury Park, CA 91320 • (805) 375-6600 • Fax: (805) 375- 6602 • www.point9.com • www.rfmosfet.com

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter		Test Conditions			Min.	Typ.	Max.	Unit
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0	I_D = 100mA		70			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 28V	V_{GS} = 0				6	mA
I_{GSS}	Gate Leakage Current	V_{GS} = 20V	V_{DS} = 0				1	μA
$V_{GS(th)}$	Gate Threshold Voltage*	I_D = 10mA	V_{DS} = V_{GS}		1		7	V
g_{fs}	Forward Transconductance*	V_{DS} = 10V	I_D = 6A		4.8			S
G_{PS}	Common Source Power Gain	P_O = 150W			13			dB
η	Drain Efficiency	V_{DS} = 28V	I_{DQ} = 0.6A		50			%
VSWR	Load Mismatch Tolerance	f = 175MHz			20:1			—
C_{iss}	Input Capacitance	V_{DS} = 0V	V_{GS} = –5V	f = 1MHz			360	pF
C_{oss}	Output Capacitance	V_{DS} = 28V	V_{GS} = 0	f = 1MHz			180	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 28V	V_{GS} = 0	f = 1MHz			15	pF

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle ≤ 2%

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

THERMAL DATA

$R_{THj–case}$	Thermal Resistance Junction – Case	Max. 0.8°C / W

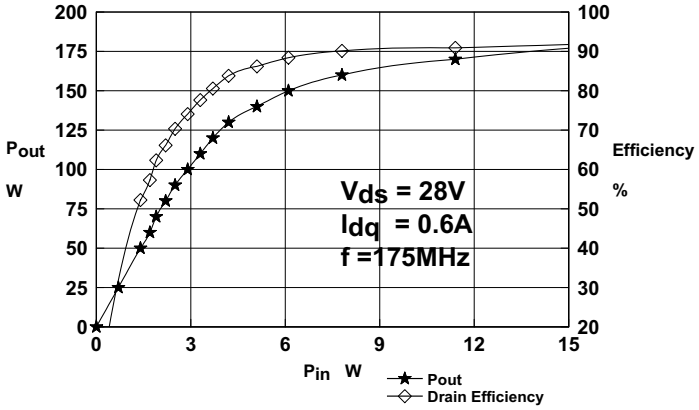


Figure 1
Power Out & Efficiency vs Power Input

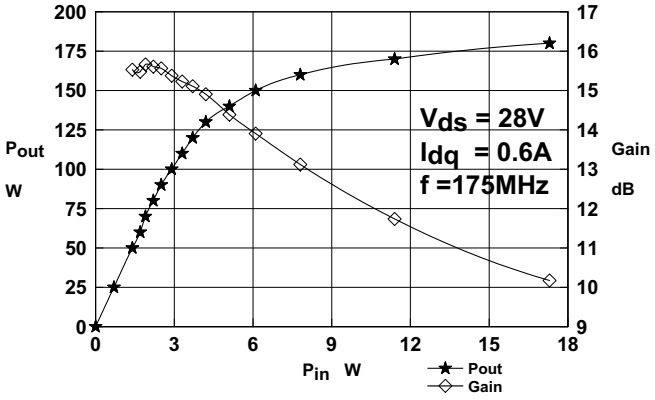


Figure 2
Power Out & Gain vs. Power Input

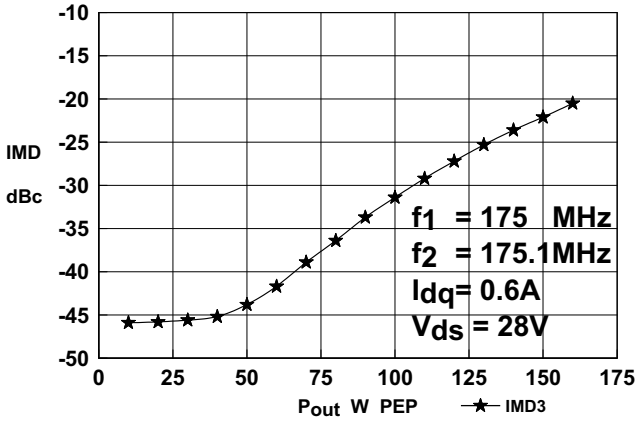
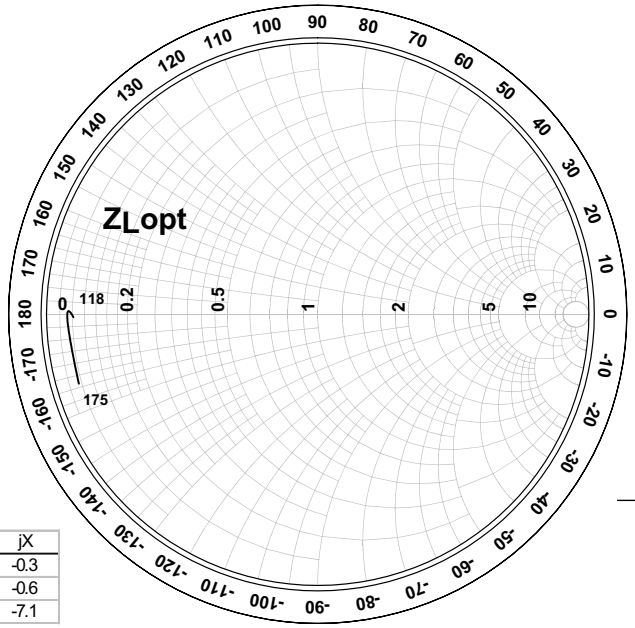


Figure 3
IMD Versus Power Output

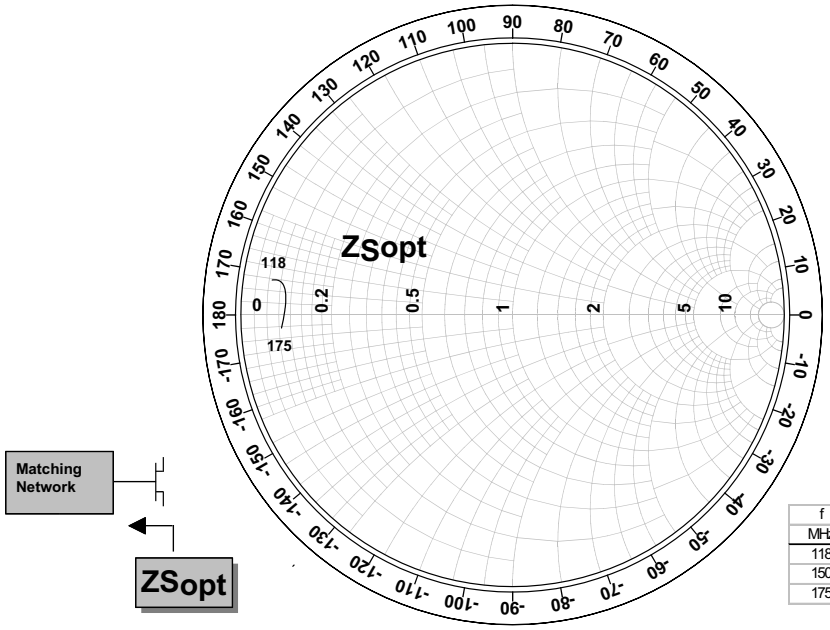
Typical S Parameters

! Vds=28V Idq=0.6A
MHZ S MA R 50

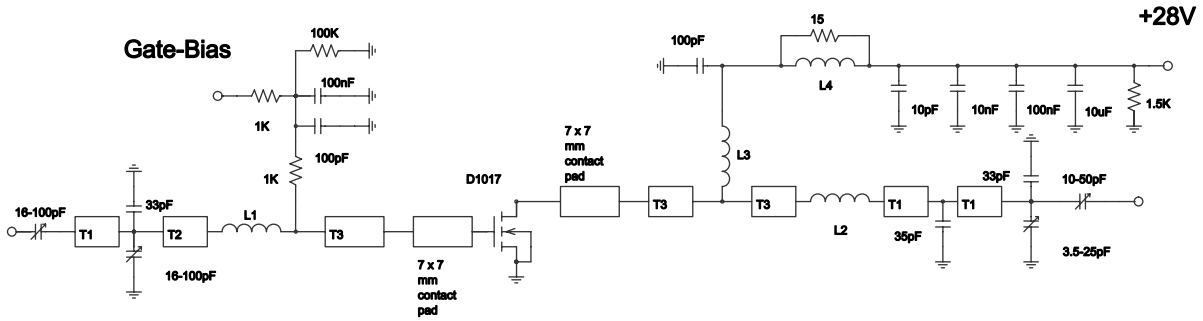
!Freq	S11		S21		S12		S22	
!MHz	mag	ang	mag	ang	mag	ang	mag	ang
50	0.83	-167.4	7.42	93.3	0.009	26.5	0.79	-167
100	0.89	-169.4	3.56	64.1	0.008	44.1	0.82	-163.7
150	0.93	-169.3	2.05	45.2	0.01	75.4	0.87	-164.7
200	0.95	-170.1	1.23	34.2	0.016	88.2	0.91	-166.3
250	0.96	-170.2	0.85	26	0.023	89.1	0.94	-167.7
300	0.97	-169.7	0.62	22.6	0.03	90.1	0.96	-169
350	0.97	-170.4	0.44	15.2	0.035	86.1	0.96	-169.8
400	0.98	-169.3	0.35	17.8	0.043	85.2	0.97	-170.5
450	0.98	-169	0.27	15.9	0.046	84	0.98	-171.7
500	0.99	-168.5	0.23	19.6	0.053	83.1	0.99	-171.4



MHz	R	jX
118	2.6	-0.3
150	2	-0.6
175	2.2	-7.1



f	ZS	
MHz	R	jX
118	2.8	3.6
150	4.3	2.7
175	4	-1.4



175MHz TEST FIXTURE

Substrate 1.6mm PTFE/glass, Er=2.5
All microsptrip lines W = 5mm

T1,T2	**7.5mm**
T3	**6mm**
L1	**Hairpin loop 18swg 10mm high, 6.5mm gap**
L2	**Hairpin loop 5mm wide ribbon, 7mm high, 3.5mm gap**
L3	**9 turns 19swg enamalled copper wire, 6mm i.d.**
L4	**12 turns 19swg enamelled copper wire on Fair-Rite FT82 ferrite core**

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*D1017

*PSPICE MODEL FOR POINT NINE RF N-CHANNEL VERTICAL DMOS POWER FET
*May 2004


*                  ____GATE
*                  I   ____DRAIN
*                  I   I   ____SOURCE
*                  I   I   I
.SUBCKT D1017  10  20  30
*Cin1,Cin2 & Lin model the input side of the package
Cin1   10    30    0.45p
Lin    10    11    0.68n
Cin2   11    30    0.45p
LG     11    12    0.2n    ;Gate bond wire inductance
CGS    12    13    276p    ;Gate-source capacitance
MOS    14    12    13      13  D1017 L=0.9U W=0.336    ;D G S B LEVEL1
JFET   16    13    14      D1017                       ;D G S
DBODY  13    16    D1017                               ;P N
LS     13    30    0.4n    ;Source bond wire inductance
CGD    12    16    6p    ;Gate-drain feedback capacitance

*Cout1,Cout2 & Lout model the output side of the package
Cout1   16    30    1.2p
Lout    16    20    1.68n
Cout2   20    30    1.2p

.MODEL D1017  NMOS (VTO=4.76 KP=2.811E-5 LAMBDA=0.032 RD=0.013 RS=0.051)
.MODEL D1017  NJF  (VTO=-4.3 BETA=1.5 LAMBDA=0.54)
.MODEL D1017  D    (CJO=493.2P RS=0.25 VJ=0.7 M=0.35 BV=75)


.ENDS
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